

# Towards Practical Reversible Logic

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## Introduction

There is now a fairly extensive literature on reversible computation[1, 2, 3, 4] which shows that the energy dissipation per device operation cannot be reduced below  $\ln(2) kT$  (where  $k$  is Boltzman's constant and  $T$  is the temperature) if the device is not reversible.

For the last 50 years the energy dissipation per gate operation has been declining with remarkable regularity[5]. Extrapolation of this trend shows the energy dissipation per device operation reaching  $kT$  (for  $T = 300$  K) by the year 2015. To gain some perspective on this consider that an "AND" gate which has a power supply of one volt and which allows a single electron to go from that one volt supply to ground during the course of a switching operation will dissipate one electron volt. Although one electron volt is about forty times  $kT$  (and well above the theoretical limit), it will be difficult to reach even this level of energy dissipation. Extrapolating present trends, we should reach forty  $kT$  between the year 2000 and 2010, e.g., within ten to twenty years.

Computers in the 21st century are expected to have a very large number of logic devices[6]. Even if we only dissipate  $kT$  per logic operation, a future computer operating at room temperature and at a frequency of one gigahertz which had  $10^{18}$  logic gates packed into a cubic centimeter would dissipate roughly four megawatts. The drive for ever greater computational power with ever more densely packed logic elements will eventually require that a single logic operation dissipate at least several orders of magnitude *less* than  $kT$ .

One of three things will occur: (a) the historic rate of decreasing energy dissipation per device operation will slow or halt in the next one or two decades or (b) we will operate computers at lower temperatures or (c) we will pursue methods of computing that use reversible logic devices in a reversible way that can beat the  $kT$  barrier.

The first option is quite unattractive. The heroic cooling methods used in the Cray 3 supercomputer to remove the heat generated by the computer's operation suggest that failure to reduce energy dissipation per gate operation would be a major limiting factor in future computer performance. Further, although the raw cost of electrical power is

not yet a major limitation, it would become so in the future if reductions in energy dissipation did not keep pace with advances in other areas.

The second option will not reduce overall energy dissipation. If we operated future devices at 3 Kelvins we would reduce  $kT$  by a factor of 100 and so could reduce energy dissipation by a similar factor - but for fundamental thermodynamic reasons the coefficient of performance of the refrigerator for the system can be at best  $3K/(300K - 3K) = 0.01$ [7]. Thus, the lower energy required per gate operation will be almost exactly balanced by the increased energy needed by the refrigerator. In many applications refrigeration is not a reasonable option. Lap top computers, embedded systems, various "smart" appliances and other applications make refrigeration undesirable.

Finally, and most attractively, we could use reversible computation to reduce energy dissipation. This would, in principle, allow energy dissipations indefinitely below  $kT$  per logic operation. While *some* barrier should eventually be encountered, the use of reversible logic should allow us to continue current trends in energy dissipation per logic operation for the longest possible time. Further research in this area is the most appropriate response to the rather limited range of possibilities that face us.

## Reversible Devices

While many proposals for reversible computation have been advanced, existing electronic devices can support reversible computation and achieve remarkably low energy dissipations. This includes CMOS transmission gates used in an appropriate way, some types of pass logic and hot clock nMOS[8], and a new reversible logic proposal combining CCDs and FETs[9].

Conceptually, all these proposals require that switching elements be "preset" before current is allowed to flow through them. Closing a switch when there is a voltage across it must be forbidden. The rush of current through the resulting short circuit would be highly dissipative. When current does flow it must do so gradually and gently. Like a river flowing evenly in its bed or water being poured gently from one cup into the next, the flow of electrons must take place with minimal turbulence. Sharp drops, like Nia-

gra Falls, must be avoided.

Helical logic[10] is a recent and very elegant proposal which provides the electronic equivalent of a switch gate. Switch gates implemented from billiard balls have been known for some time[2]. Figure 1 illustrates a switch gate.

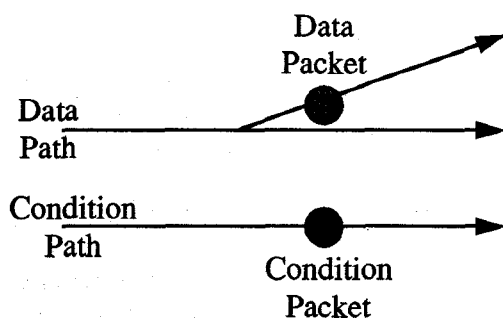


Figure 1.  
a Switch Gate

There are two incoming paths and three outgoing paths. One incoming path, the condition path, simply continues straight through. The other incoming path, the data path, splits into two outgoing branches. The switch gate operates by diverting the billiard ball on the incoming data path to one of the two outgoing paths conditional on the presence or absence of a billiard ball on the condition path. This simple operation can be used to implement a Fredkin gate, and hence is logically complete[2].

For a switch gate to work some restoring force must keep the billiard balls moving along their paths in the proper positions.

In helical logic, we control the motion of charge packets (instead of billiard balls) by placing them in helical paths and applying an electric field at right angles to the axis of the helix. The electric field confines the charge packet to a single fraction of a helical turn. As the field rotates, the charge packet is moved along the helix much as water is moved by an Archimedes screw. The rotating electric field provides both the power to move the charge packet and the clock to synchronize the motion of many charge packets. Multiple helical paths can carry multiple charge packets.

This electronic switch gate operates by bringing together two helical paths and, just as in the conventional switch gate, splitting one of the helical paths into two outgoing helical paths. By properly designing the geometry of the switch gate the charge packet in the data path can be steered into the correct outgoing path by the presence or absence of charge in the condition path.

Helical logic has a number of desirable properties. First, the logic operations are thermodynamically reversible and asymptotically non-dissipative. By slowing the speed of

operation, energy dissipation per logic operation can be made as small as desired. Second, the rotating electric field (which could be provided by a cavity resonator) provides both clock and power. This eliminates the need to charge and discharge clock lines. By making the computational device from materials with low dielectric loss factors energy dissipation can be made very small, particularly at low temperatures. There is also no need to waste space on clock and power lines: every point in the circuit is bathed in an electric field that provides both. Third, charge transport is both very efficient (in terms of energy dissipation) and can be controlled. By increasing or decreasing the radius of curvature of the helices, the speed at which charge is transported can be adjusted to suit the needs of the particular circuit. If slow charge transport is sufficient for the particular logic function, then helices with a small radius of curvature can be employed. If rapid charge transport is required, larger helices can be used. Varying the geometry of the helices will produce a wide range of specific charge transport properties.

While it might seem that helical logic is inherently three dimensional (and hence difficult to manufacture with current technology) it should be feasible to implement a planar variation of it[10]. The near term practicality of this method requires further research.

Further research in minimally dissipative elements is required if electronic devices are to reach the packing densities that are achievable.

## References

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